Venu Gopal

Senior IC Layout Consultant

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About me

Dynamic, Highly experienced IC Layout Consultant with 21+ years of proven success in delivering first-time-right silicon across RF, High Performance Analog, and Automotive domains. Adept at managing complex layout projects, from block-level to full-chip, with deep expertise in top-down design methodologies, EM/IR optimization, and process node mastery from 20nm to 350nm. Known for precision, reliability, and leadership — having directed teams, created layout QA protocols, and collaborated with top semiconductor companies globally. Passionate about technology, quality, and continuous improvement.

Tools & Languages

- Layout Tools: Virtuoso, Virtuoso-XL, OpenAccess
- Verification Tools: Chameleon (LVS), Assura, Calibre, Hercules (DRC, LVS, Antenna checks, and custom rule files)
- Auto-Routing Tools: IC Craftsman (VCR)
- Programming Languages: C++, PERL, UNIX Shell Scripting, SKILL

Experience Summary

- Analog/Mixed-Signal, RFIC, Automotive, Low-Power Layout Engineer with deep specialisation
- 21+ years of experience in high-speed, EM-tested, high-current RF/analog layout environments
- Comprehensive expertise across all layout design stages, with roles ranging from layout engineer to principal engineer and team lead
- 5 years of focused experience in RF/analog layout working environments
- 6 years of experience mentoring layout teams of 2–8 engineers
- End-to-end layout execution from IP floor-planning to GDSII tape-out at both IP and full-chip levels, excelling as both team player and team lead
- Highly motivated and committed to tape-out quality with minimal iterations
- Delivered 200+ block layouts |2 EM STD Cell Libs | 30+ mega module layouts | 30+ test chip tape-outs | 10+ full chip tape-outs
- Specialised in: High-Speed (10–20GHz), High-Current (1A+), RF/Analog designs
- Process node experience across: TSMC / GF / CSM / INF / ACTEL / TI / NXP
- 20nm SOI | 40nm | 65nm / 90nm | 130nm | 180nm | 250nm | 350nm
- Tools and platforms: Virtuoso-XL and GXL | Calibre | Assura | Pegasus | ADE Maestro | Voltus-Fi | EM/IR Analysis
- Worked with: Qualcore Logic Ltd, Wipro-Newlogic, Qimonda, Infineon, Texas Instruments, Sensor Dynamics, SiTel Semiconductors, NXP, Philips, ST-NXP, and ST-Ericsson

Technical Experience Highlights

- Analog Blocks: Bandgap Reference, High Voltage Regulators, Sense Amplifiers
- Flash Memory: Array and Periphery Sub-Blocks
- Digital Blocks: Y-Mux, Data-Mux
- Process Nodes: 0.25µm, 0.18µm, 130nm, 90nm, 65nm, 60nm, 48nm,22nm
- Metal Stacks: 3LM, 6LM, 8LM with Multi-Poly,10 LM
- Foundries: TI, TSMC, NXP, CSM, Infineon, Tower, IBM, ROHM
- Processes: Triple-Well, Dual-Well, High-Performance Analog, RF Layout, Digital CMOS
- Full-Chip Layout: High-Speed USB (incl. Digital PLL, DLL)
- RF Transceivers (5+): DCO, PA, LNA, Mixer, Divider, Bias Circuits, Power Management Units
- Top-Level Integration: RF System Layout and Validation

Projects Summary

Texas Instruments

2010–Present

DAC & ADC

- Responsible for full top-level layout of modules like dac_top across three different chips
- Contributed to sub-blocks in ADCs, reference top levels (ref_top), and all high-speed/high-current analog sections
- Target frequencies ranged from 10 GHz to 23 GHz
- Process nodes: 20nm, 48nm, and 65nm DSM (TI internal, TSMC, GF)
- Tools and Flow:
- Assura & Pegasus (DRC/LVS)
- TI internal tools for layout verification
- Assura QRC for parasitic extraction
- Quantus, Voltus-Fi, and ADE for EM/IR analysis

DC-DC Converters

- Responsible for layout and verification of IPs for low-power DC-DC sub-blocks
- Key blocks: Bias blocks, Bandgap References, Voltage Regulators, Operational Amplifiers (OpAmps), Sensors, and Chip Top Levels
- Specialized in DC-DC converter layouts with output currents up to 1A
- Tools and Flow: Assura (DRC/LVS), OpenAccess, and TI internal verification tools
- Delivered custom layout and physical verification with minimal iterations

RFID

- Led the padring layout and floorplanning at both block and module levels, including pin assignments for digital integration and layout of critical analog/RF blocks.
- Delivered RF superheterodyne receiver layouts for both 2.4 GHz BLE and 900 MHz applications.
- Served as RF Layout Team Lead for 4–10 layout engineers over 4 years, managing all RF layout activities, including LNA, Mixer, and LDO designs.
- Developed and implemented complex layout methodologies to meet stringent design and performance requirements.
- Acted as the primary liaison between layout and design teams, ensuring clear communication and efficient collaboration.
- Consistently met demanding deadlines through effective coordination and leadership.
- Completed 6 full chips:
  - 3 LF chips for Automotive Base Stations
  - 2 Immobilizer ICs
  - 2 BLE/LF Transceiver chips
- Delivered 10 test chips to validate standalone IPs, including PLLs up to 5 GHz.

Education :

- Special Diploma in Electronics with Specialization in Communications (10+3.5 years)

Hobbies

- Web Development – HTML/CSS, Netlify, and domain setups.
- Photography & Visual Media – photo aesthetics.
- Travel & Cultural Exploration – Visited 50+ countries and adjusting to multiple work cultures.
- Mentoring & Team Leadership – mentoring junior engineers and team collaboration
- Erasmus Student Support Volunteer

References

- Available upon request.

Projects Summary (CONT)

Philips & NXP Wireless (Nijmegen, NL)

May 2008 – Apr 2010

- 40nm RF CMOS process
- LNA, MIXER, DIVIDER, Bias, Power Supply
- DC-DC Converter
- Analog Attenuator (Full Chip)
- 6GHz Tunable VCO (3-Band, Full Chip)
- RX Front-End IP Integration

Wipro Newlogic (Munich, DE)

Mar 2008 – May 2008

- CMOS 0.18µm, 0.13µm
- Layout migration and process adaptation
- DAC and Modulator/Demodulator layout and verification

SiTel Semiconductors (Den Bosch, NL)

Mar 2008 – May 2008

- 0.18µm RF analog layout
- Power Amplifier (PA) sub-blocks (Custom/Semi-Custom/Mixed-Signal)
- Multiple PA versions for Test Chips

Infineon & Qimonda Flash (Munich, DE)

Mar 2006 – Dec 2007

- 36nm PCRAM Memory
- JDI Column Variants with Matching Techniques
- Bandgap Reference, Voltage Regulator (48nm & 60nm)
- Register Banks (128-bit), Comparators, OPAMPs
- Y-Mux, Data-Mux
- High Voltage Analog & Digital Control Blocks
- Full Memory Integration with IR Drop/Electro-Migration Checks

TI Offshore Design Center (Hyderabad, IN)

Jan 2005 – Mar 2006

- TI ODC RF Team: LNA, Mixer, LDO (90nm & 65nm)
- Team Lead (8 members), Layout Methodology Creation
- TI ODC High Performance Analog Team:
- RF & Baseband for Mobile Radios, USB Chips , Receiver Mega Module
- Team Player and Team Lead (6+ months)

Qualcore Logic Ltd (Hyderabad, IN)

Mar 2004 – Jan 2005

- Nodes: 90nm, 0.18µm, 0.25µm, 0.35µm
- Foundries: TSMC, CSM, Infineon, Tower, UMC, Rohm
- High-Speed USB (PLL, DLL, DAC, ADC)
- Image Sensors, On-Chip Monitors
- Mega Module Test Chip Integration